CLAIM AMENDMENTS

1. (Currently Amended) A method for characterizing a circuit described by a logic model, wherein the circuit includes a plurality of registers wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever clocked by a succession of clock signal edges, and wherein the circuit also includes circuit logic controlling the state of each register input signal in logical response to circuit input and register output signals, the method comprising the steps of:

a. processing the logic model to perform a simulation of circuit behavior thereby producing waveform data indicating states of circuit input and register output signals as functions of time;

b. processing the logic model to generate a plurality of net models, each net model corresponding to a separate one of the registers and depicting a logical relationship between the register's input signal and all others of the circuit input and register output signals that influence a state of the corresponding register's input signal between clock signal edges; and

c. generating a display including a plurality of register symbols arranged in a plurality of columns,

wherein each column corresponds to a time of occurrence of a separate one of the clock signal edges,

wherein each register symbol ~~indicating~~ indicates a state of a register output signal produced by a corresponding register after being clocked by a ~~pulse~~ clock signal edge at a time corresponding to a column in which the register symbol resides as indicated by the waveform data,

wherein the display also includes a graphical representation of a logical relationship depicted by ~~at least~~ one of the net models visually linking one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns, and

wherein the graphical representation indicates that a register output signal state indicated by the one register symbol, and states of register output signals indicated by the other register symbols are logically interrelated.

2. (Currently Amended) The method in accordance with claim 1 wherein ~~each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges~~ the state of the register output signal indicated by the one register symbol is a function of the state of the register output signals indicated by the other register symbols.

3. (Currently Amended) The method in accordance with claim 1 wherein the ~~representation of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols~~ states of the register output signals indicated by the other register symbols are functions of the register output signal indicated by the one register symbol.

4. (Currently Amended) The method in accordance with claim 1 wherein the display also includes a plurality of circuit input signal symbols arranged in at least one of the columns, each circuit input signal symbol depicting a state of a circuit input signal at a ~~separate~~ time corresponding to a column in which the circuit input signal symbol resides ~~during the simulation~~, and

wherein the graphical representation visually links the one register signal symbol to at least one of the other register signal symbols and to at least one of the circuit input signal symbols.

5. (Canceled)

6. (Currently Amended) The method in accordance with claim 4 wherein the graphical representation ~~of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols and of a state of an input signal depicted by one of the displayed input signal symbols~~ also indicates that the register output signal state indicated by the one

register symbol is a logical function of states of register output signals indicated by the other register symbols and the state of at least one of the circuit input signals.

7. (Currently Amended) The method in accordance with claim 1 wherein the graphical representation of a logical relationship comprises ~~a line interconnecting two of the register symbols~~ lines visually linking the one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns.

8. (Currently Amended) The method in accordance with claim 1 wherein the display of the graphical representation of a logical relationship also comprises a graphical representation of one of the net models visually linking ~~two of the registers~~ the circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol.

9. (Currently Amended) The method in accordance with ~~claim 4~~ claim 6 wherein the representation of a logical relationship comprises ~~a graphical representation of one of the net models linking two of the registers~~ lines interconnecting the one register symbol to the other register symbols and at least one of the circuit input signal symbols.

10. (Currently Amended) The method in accordance with ~~claim 4~~ claim 6 wherein the graphical representation of a logical relationship comprises a graphical representation of one of the net models ~~wherein the graphic representation indicates how an input signal state depicted by one of the input signal symbols logically influences~~ visually linking the circuit input signal symbol and the other register symbols to a register input signal symbol depicting a state of a register input signal corresponding to ~~one displayed register symbol~~ the one register symbol.

11. (Currently Amended) The method in accordance with ~~claim 10~~ claim 2

~~wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges, and~~

~~wherein each input signal symbol is horizontally positioned in the display to represent the time at which the input signal is of the depicted state~~

wherein a distinguishable graphical representation visually linking the other register symbols to the one register symbol indicates a changed state of the other register symbol after being clocked by a clock signal edge at a time corresponding to a column in which the other register symbol resides.

12. (Currently Amended) A method for characterizing a circuit ~~including a plurality of registers and other logic, wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever~~ clocked by a succession of clock signal edges, and ~~wherein the other logic controls the state of each register input signal in logical response to circuit input and register output signals~~ receiving and generating a plurality of data signals that change state at times controlled by the clock signal edges, the method comprising the steps of:

a. displaying a plurality of ~~register~~ columns of symbols,

wherein each column corresponds to a time of occurrence of a separate one of the clock signal edges

wherein each ~~register~~ symbol within each column ~~indicating~~ indicates a state of a ~~register output produced by a corresponding register after being clocked by a pulse signal edge~~ separate one of said signals at the time corresponding to the column ~~as indicated by the waveform data, wherein a horizontal position of each register symbol represents a time of occurrence of a pulse signal edge~~; and

~~b. displaying a plurality of input signal symbols, each indicating a state of the input signal at a separate time indicated by a horizontal position of the input signal system;~~ ~~c. displaying a representation of logic interconnecting the register symbols and the input signal symbols indicating how indicated states of input signals and register output signals influence states of register input signals~~

b. displaying a graphical representation visually linking one symbol residing in one of the columns to others of the symbols residing in another of the columns,

wherein the graphical representation indicates that a state of a

data signal indicated by the one symbol, and states of data signals indicated by the others of the symbols are logically interrelated.

13. (Currently Amended) An apparatus for characterizing a circuit described by a logic model, wherein the circuit includes a plurality of registers wherein each register sets a state of a corresponding register output signal to match a state of a corresponding register input signal whenever clocked by a succession of clock signal edges, and wherein the circuit also includes circuit logic controlling the state of each register input signal in logical response to circuit input and register output signals, the apparatus comprising:

a logic synthesizer for processing the logic model to perform a simulation of circuit behavior thereby producing waveform data indicating states of circuit input and register output signals as functions of time;

means for processing the logic model to generate a plurality of net models, each net model corresponding to a separate one of the registers and depicting a logical relationship between the register's input signal and all others of the circuit input and register output signals that influence a state of the corresponding register's input signal between clock signal edges; and

means for generating a display including a plurality of register symbols arranged in a plurality of columns,

wherein each column corresponds to a time of occurrence of a separate one of the clock signal edges,

wherein each register symbol ~~indicating~~ indicates a state of a register output signal produced by a corresponding register after being clocked by a ~~pulse~~ clock signal edge at a time corresponding to a column in which the register symbol resides as indicated by the waveform data,

wherein the display also includes a graphical representation of a logical relationship depicted by ~~at least~~ one of the net models visually linking one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns.

wherein the graphical representation indicates that a register output signal state indicated by the one register symbol, and states of register output signals indicated by the other register symbols are logically interrelated.

14. (Currently Amended) The apparatus in accordance with claim 13 wherein ~~each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges~~ the state of the register output signal indicated by the one register symbol is a function of the state of the register output signals indicated by the other register symbols.

15. (Currently Amended) The apparatus in accordance with claim 13 wherein the ~~representation of a logical relationship comprises data included in the display indicating that a state of a register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols~~ states of the register output signals indicated by the other register symbols are functions of the register output signal indicated by the one register symbol.

16. (Currently Amended) The apparatus in accordance with ~~claim 14~~ claim 13

wherein the display also includes a plurality of circuit input signal symbols arranged in at least one of the columns, each circuit input signal symbol depicting a state of a circuit input signal at a ~~separate~~ time ~~during the simulation~~ corresponding to a column in which the circuit input signal symbol resides, and

wherein the graphical representation visually links the one register signal symbol to at least one of the other register signal symbols and to at least one of the circuit input signal symbols.

17. (Canceled)

18. (Currently Amended) The apparatus in accordance with claim 16 wherein the graphical representation ~~of a logical relationship comprises data included in the display indicating that a state of a~~

~~register input signal of a register corresponding to one of the displayed register symbols is a logical function of a state of a register output signal of a register corresponding to at least one other of the displayed register symbols and of a state of an input signal depicted by one of the displayed input signal symbols~~ also indicates that the register output signal state indicated by the one register symbol is a logical function of states of register output signals indicated by the other register symbols and the state of at least one of the circuit input signals depicted by a circuit input signal symbol.

19. (Currently Amended) The apparatus in accordance with claim 13 wherein the graphical representation of a logical relationship comprises ~~a line interconnecting two of the register symbols~~ lines visually linking the one register symbol of the register symbols residing in one of the columns to other register symbols residing in another of the columns.

20. (Currently Amended) The apparatus in accordance with claim 13 wherein the display of the graphical representation of a logical relationship also comprises a graphical representation of one of the net models visually linking ~~two of the registers~~ the circuit logic depicted by at least one of a plurality of logic gate symbols to the one register symbol.

21. (Currently Amended) The apparatus in accordance with ~~claim 17~~ claim 18 wherein the representation of a logical relationship comprises ~~a first line interconnecting a first one of register symbols to a second one of the register symbols and a second line interconnecting the first one of the register symbols to one of the input signal symbols~~ lines interconnecting the one register symbol to the other register symbols and at least one of the circuit input signal symbols.

22. (Currently Amended) The apparatus in accordance with ~~claim 17~~ claim 18 wherein the graphical representation of a logical relationship comprises a graphical representation of one of the net ~~models, wherein the graphic representation indicates how an input~~

~~signal state depicted by one of the input signal symbols logically influences~~ models visually linking the circuit input signal symbol and the other register symbols to a register input signal symbol depicting a state of a register input signal corresponding to ~~one displayed register symbol~~ the one register symbol.

23. (Currently Amended) The apparatus in accordance with ~~claim 22~~ claim 14

~~wherein each register symbol is horizontally positioned in the display to represent timing of one of the clock signal edges, and~~

~~wherein each input signal symbol is horizontally positioned in the display to represent the time at which the input signal is of the depicted state~~

wherein a distinguishable graphical representation visually linking the other register symbols to the one register symbol indicates a changed state of the other register symbol after being clocked by a clock signal edge at a time corresponding to a column in which the other register symbol resides.

24. (Currently Amended) An apparatus for characterizing a circuit ~~described by a circuit logic model as having a set of~~ clocked ~~registers interconnected by un-clocked logic,~~ by a succession of clock signal edges and receiving and generating a plurality of data signals that change state at times controlled by the clock signal edges, the apparatus comprising:

~~a circuit simulator for processing the circuit logic model to produce waveform data indicating states of circuit input signals and of register output signals as functions of clock signal edge timing; and~~

~~means for processing the waveform data and the logic model to produce a temporal schema model characterizing the circuit's logic and behavior, and~~

~~means for producing a display based on the temporal schema model using separate symbols to represent successive circuit input signal states and successive register output signal states relative to various clock signal edges during the simulation behavior, wherein the display also graphically depicts fan-in or fan-out logical~~

~~relationships by which circuit input signal states and register output signal states influence register input signal states~~

a means for generating a display of a plurality of columns of symbols,

wherein each column corresponds to a time of occurrence of a separate one of the clock signal edges,

wherein each symbol within each column indicates a state of a separate one of said data signals at the time corresponding to the column; and

a means for generating a display of a graphical representation visually linking one symbol residing in one of the columns to others of the symbols residing in another of the columns, wherein the graphical representation indicates that a state of a data signal indicated by the one symbol, and states of data signals indicated by the others of the symbols are logically interrelated.